Integrated Methods to Detect and Locate Electrical Continuity and Leakage: A Bayes Approach

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Abstract

This paper presents an integrated methodology to detect and locate electrical continuity and leakage between and within two groups of nets. Skilling (1982) addressed the leakage problem and patented a clever method with complexity of O(n). By using group testing methods, Chen and Hwang (1989) improved complexity to $O(\log_2 N)$ for integrity test for circuit board, and Chen and Chen (2011) introduced the statistical method to further reduce the number of tests required to detect and locate leakage. In this paper, we extend Chen and Chen's (2011) method to address both leakage and continuity problems. Based on Bayesian techniques, we now present an integrated testing methodology to incorporate circuit topological information and a defective database into the testing algorithm to reduce the number of required tests. Furthermore, we conclude that the presented integrated methodology can be implemented by most commercial test equipment.

Key Words: Bayes estimation, High voltage break down test, Continuity fault, leakage faults.

I. Introduction

Due to voltage surge in telephone lines connecting the residential and the telephone switching system, which might occur during lightning, the interface circuit board, known as the Line Unit Circuit in the switching system, has a circuit board designed to resist up to 365 volts and hence the need to perform a break down test for 1000 volt during the manufacturing test. This poses a challenge to the circuit designer and switching system manufacturer since testing for high voltage circuits is time consuming and expensive.

High voltage break down circuit testing is known to be time consuming and expensive. For instance, depending on features and support, a test equipment such as Faichild-70 used in the AT&T Oklahoma City Plant ranges from 1 - 1.5 million dollars. In addition to the equipment costs, and the cost of an engineer is needed to perform circuit test and the test equipment maintenance.

Thus, the objectives of high-voltage testing problem are two-fold:

1. To verify the circuits are free of fault.
2. To detect and locate which pair(s) of nets are shorted. (See Figure 1 below)

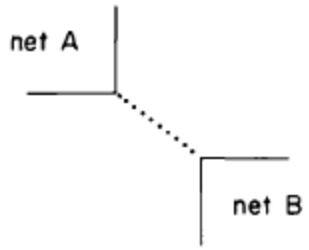

Fig. 1. A diagonal short between two nets.

In this article, we propose to speed up the testing time by utilizing the Bayes/Empirical Bayes statistical method to incorporate the testing defect data and circuit topological structure. Specifically, we will develop a statistical-based testing algorithm to speed up the fault detection and fault localization algorithms and hence reduce the testing cost.

Preliminary results indicate the benefit of this proposed approach, and that the new approach is publishable and may even be patented should the patent application costs be given support.

Specifically, the results indicate that the number of test required

was reduced significantly as follows:

1. Complexity of fault detection algorithm. The number of test required T: $1 \le T \le \log_2 \chi(G)$; where $\chi(G)$ is the chromatic number of graph G with $p_{ij} > 0$

2. And fault localization tests required:

$$d \le T \le 2d \log_2 \chi(G);$$

where N is chromatic number of graph of the network under test with $p_{ij} > 0$;

and d be the number of shorted pair of nets.

II. Review of Literature

Exiting research performed in this problem can be summarized as follows:

- Skilling (1982) US Patent 4 342 959, Aug. 3, 1982. Using linear algorithm O(n). Used in Faichild-70 series in circuit test set and other commercial test equipment

- Group Testing techniques: First invented during World War II for detecting VD among US GIs. Chen & Hwang (1989] invented a combinatorial test using group testing concept with complexity of $O(\log_2 N)$ published in IEEE Transactions on Circuit and System in 1989.

- Chen & Chen (2011) proposed leakage test algorithm using Bayes method.

Notice that except for Chen and Chen's (2011) approach, all the mentioned approaches are based on deterministic approaches, and hence all pairs of circuits have an equal chance of engaging in short fault but need to be tested during the fault detection stage.

Recently, we revisited this problem and decided to further improve the performance of the circuit testing problem based on the following observations :

1. The numbers of circuits that can possibly be engaged in circuit shorts are in fact relatively few based on the defect database collected during the manufacture process, as well as circuit topology. Therefore, statistical techniques may be needed to improve the test algorithm significantly.
2. We propose using Bayes technique to incorporate the defect data and circuit topological information into the algorithm design.

III. Objectives and Proposed Methods

Consider a circuit board with ***n*** networks. Without loss of generality, we assume *n = 2".* Each network can be represented as a tree in graph terminology, and each tree can be represented a vertex in graph G. The Chromatic number, $\kappa(G)$, of graph G is the minimum number of colors such that any two adjacent vertices have different colors. Let $\kappa(G)$

the minimum number of colors such that any two adjacent vertices in G have different colors.

The objective of this paper is to design a fast and practical testing algorithm to:

1. Reduce the number of tests required to ensure the circuit board is indeed free of fault(s) using a Bayes approach
2. Speed up the test time by reducing the number of tests required to locate all faulty circuits, if any.
3. Propose an integrated testing algorithm to perform leakage and continuity test with existing commercial test equipment(s) in industry.

Consider a circuit board with ***n*** networks. Without loss of generality we assume *n = 2".* Each network can be represented as a tree in graph G. Both detection and fault localization tests are based on the incorporation of real defect database and circuit topological information using Bayes/Empirical Bayes techniques.

The proposed method can be described as follows:

Step 1: Develop the fault detection and fault localization tests based on simulated defect data and on the topological structure of the circuit board

Step 2: Summarize the simulated defect data using Bayes/Empirical Bayes approach to construct a defect probability matrix.

Step 3. Based on the estimated defect matrix to construct the potential circuit shortage graph G.

Step 4. Develop fault detection/fault localization algorithm using graph coloring methods.

Step 5. Repeat step 3 and 4 until all shorted pair(s) are located

Step 6. For each circuit perform the continuity test and identify all open circuits.

Step7: Evaluate the number of test required for both fault detection and fault localization tests.

The statistical model for each step described above is as follows: The defect probability matrix P for a circuit board with n circuits is defined as:

	N_1	N_2	N_3	N_4	N_5	N_n
N_1	0	p_{12}	p_{13}	p_{14}	p_{15}	p_{1n}
N_2		0	p_{23}	p_{24}	p_{25}	p_{2n}
N_3			0	p_{34}	p_{35}	p_{3n}
N_4				0	p_{45}	p_{4n}
N_5					0	p_{5n}
N_n						0

Figure 2: Shorted probability matrix

Where p_{ij} is the probability of net 1 shorted to net j. hence $\sum_{i=1}^{n}\sum_{j=1}^{n} p_{ij} = 1$. Clearly,

$p_{ij} = p_{ji}$ for all i,j=1,2, ..., n.

since the number of shorted pair follows a Binomial distribution with probability P.
Based on defect database and topological information structure we can estimate P based on Bayes methods with Dirichlet distribution as distribution prior probability distribution for P as follows:

$$\underline{P} \sim Dirichlet(\alpha_{12}, \alpha_{13}, ..., \alpha_{n-1,n})$$

$$f(\underline{P}) = \frac{\Gamma(\sum_{i=1}^{n} \alpha_{ij})}{\prod_{i=1}^{n} \Gamma(\alpha_{ij})} \cdot \prod_{i=1}^{n} p_{ij}^{\alpha_{ij}-1}$$

The Bayes estimator for p_{ij} is as follows:

$$\hat{p}_{ij} = \frac{\alpha_{ij} + x_{ij}}{\alpha_0 + n};$$

x_{ij} *is* the defect data for N_i shorted to N_j.

Based on the estimated probability matrix P to construct the interconnection graph G as follows:

	N_1	N_2	N_3	N_4	N_5	N_6	N_7
N_1	0	p	0	0	p	p	p
N_2		0	p	p	0	0	0
N_3			0	p	p	p	0
N_4				0	p	0	0
N_5					0	0	p
N_6						0	p
N_7							0

Figure 3: Estimated shorted probability matrix

Where the Bayes estimator for $\hat{p}_{ij}$ is presented in red. Hence, $\hat{p}_{ij} > 0$ indicates that there is a positive probability that net 1 can be shorted to net j.

Based on estimated probability matrix $\hat{P}$ we can construct the graph G as follows:

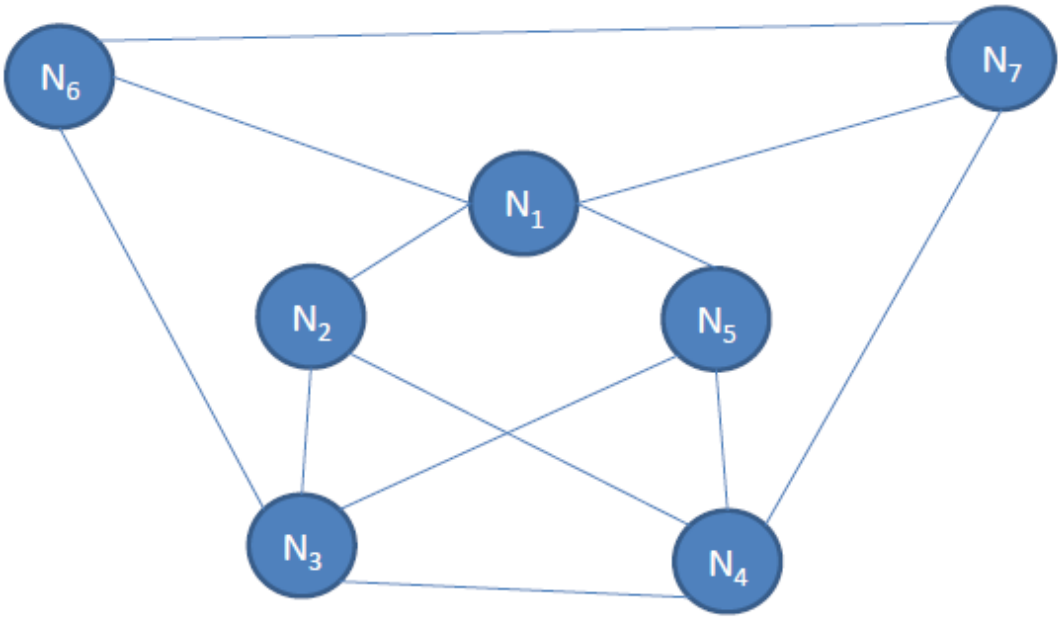

Figure 4: Estimated shortened graph G

Graph G can be portioned into κ disjoint subsets such that each that two adjacent node (nets) with distinct color. Notice that nets within the same subset (color) will not short together ($p_{ij} = 0$). Thus, the short detection algorithm was reduced to detect short pair(s) between the κ groups. Hence, the complexity of ensuring the network is free from short fault is $\log_2 \kappa$ and for detecting one shorted pair is $1 \le T \le (\log_2 (N_i + N_j) \le \log_2 N - 1;$. Where κ (named chromatic number of graph G and N_i, N_j are number of nets within group I, and j, respectively. We summarize and compare the results against Skillings (1982) and Chen and Hwang (1989) as follows:

Methods	Breakdown Test for Integrity	Short Detection	d Short pair(s) localization	Continuity Test For l defect(s)
Skilling's Method (1982)	(N-1)	(N-1)	$d \cdot (N-1)$	$l \cdot (N-1)$
C. Chen and F. Hwang (1989)	$\log_2 N$	$Log_2 N$	$d \cdot (\log_2 N - 1)$	$l \cdot \log_2 N_i$
C. Chen, R. Torres, and P. Gomez (2012)	$\log_2 \kappa$	$1 \le T \le Log_2 \kappa$	$d \cdot (\log_2 N_i + \log_2 N_j)$	$l \cdot \log_2 N_i$

Table 1: Complexity of proposed algorithm and prior algorithms: a comparison

IV. Steps in Integrated Breakdown test for continuity and leakages

The integrated high voltage breakdown test for continuity and leakage algorithm can be described as follows:

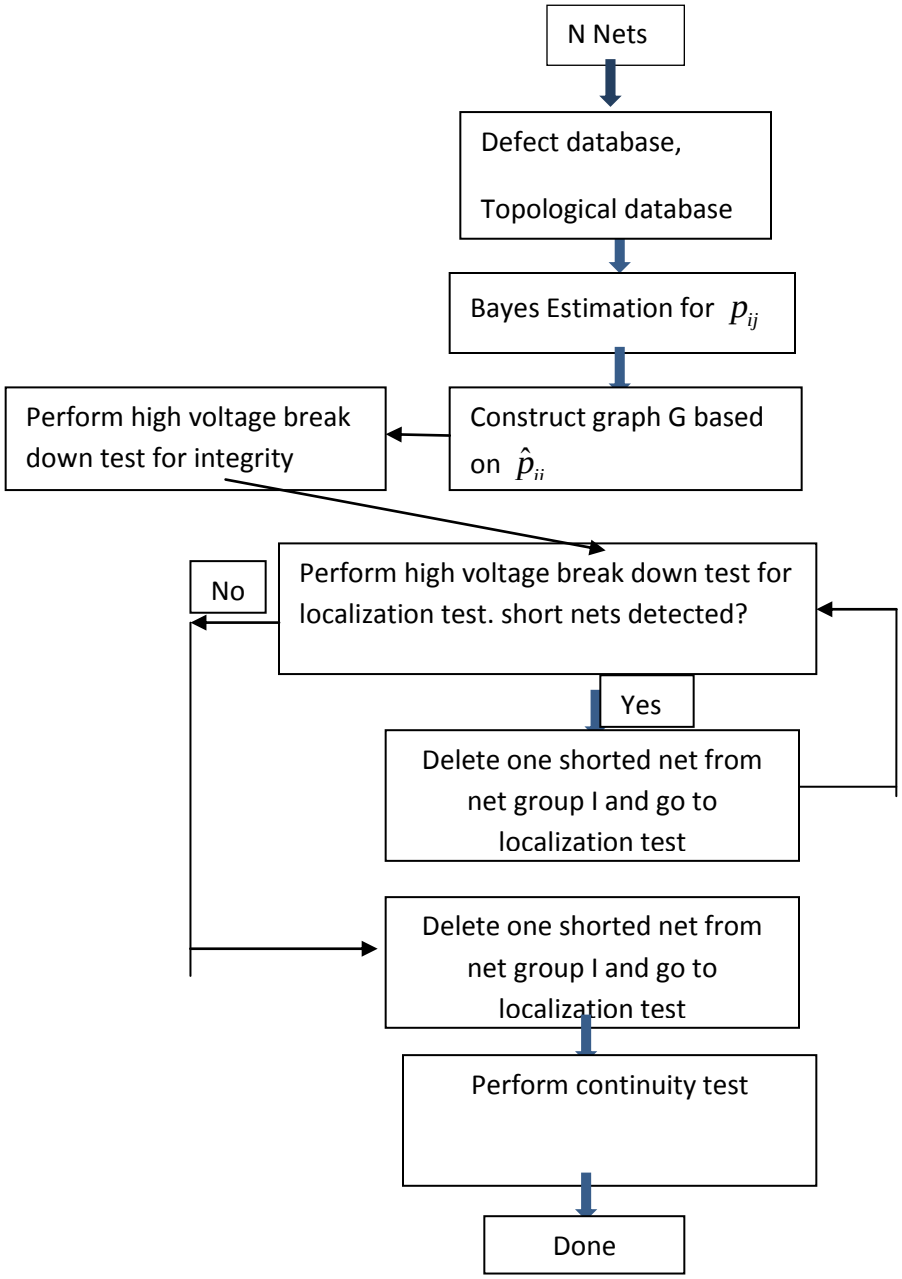

Figure 5: Proposed Algorithm

References

C. C. Chen and F. K. Hwang. “Detecting and locating electrical shorts using group testing” IEEE Transactions on Circuits and Systems, vol. 36, No. 8, 1989.

J. K. Skillings. “Method of electrical short testing and the like” US patent 4342959, Aug 3, 1982.